THE USE OF LOW POWER OPERATIONAL AMPLIFIERS IN TRACK-AND-HOLD AMPLIFIERS

by

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I. Introduction

The purpose of this report is to document the use of low slew rate operational amplifiers in the construction of sample-hold amplifiers. Conventional sample-hold theory, error sources and implementation methods will be discussed. The low slew rate track-and-hold's operation will be examined and differences from more conventional devices noted. A detailed description of several very low power track-and-hold amplifiers which are suitable for use with band- and amplitude-limited instrumentation systems is then given. This description includes discussions of all sources of error applicable to the track-and-hold amplifier. A dual channel track-and-hold amplifier system suitable for use with a 15-bit battery operated instrumentation system is then described

II. The Purpose of Sample-Hold Amplifiers

Sample-hold amplifiers are analog memory devices which reduce the aperture time of analog to digital conversion systems. Sample-hold amplifiers are used to "freeze" the analog input voltage at some instant of time. This ability to catch the analog voltage at some given instant allows the analog to digital converter system (ADC) to better approximate the Sampling Theorem's required delta sample pulses.

The non-zero width of the ADC's sampling window causes the digital output to have an envelope surperimposed on the output's frequency spectrum described by equation 2.1 [1]

$$\sin((\omega * \tau)/2)/((\omega * \tau)/2) \qquad (2.1)$$

where ω is the angular frequency and τ is the sample pulse's width. Making τ as small as possible will extend the first null of this envelope well beyond the frequencies of interest and give a flat amplitude response in the sampled spectrum's frequencies of interest. ADC's can have aperture times (sample pulse widths) hundreds of microseconds wide while sample-holds may have aperture times of only tens of nanoseconds. Figure 2.1 shows how these differing aperture times can affect the sampled data spectrum envelope.

The time required for an ADC to make a conversion can be considered as its aperture time, since this aperture time may be several hundred microseconds long, the analog input signal could change by a significant amount. The aperture time of a system can be thought of as the shutter speed of a camera. If the shutter speed is slow a fast moving object will appear blurred

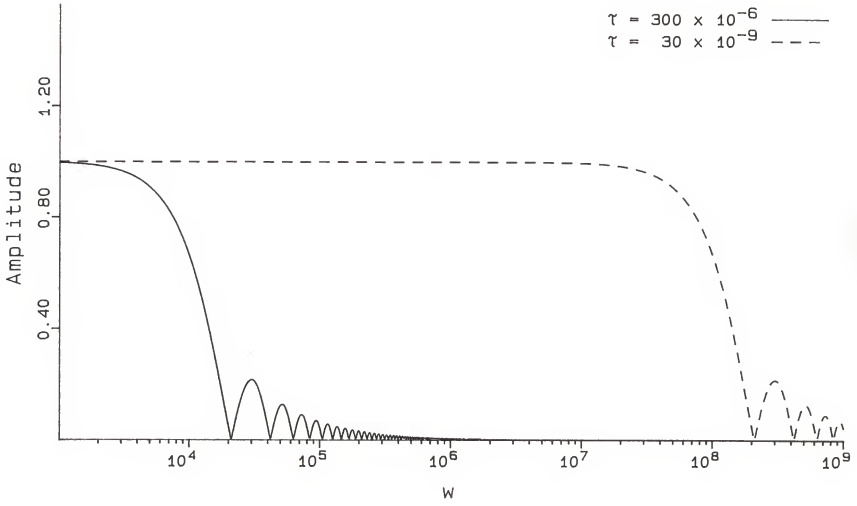


Figure 2.1. Sample data spectrum envelopes for two values of τ. (a) 300×10^{-6} and (b) 30×10^{-9}

(i.e., the motion is integrated over time), while a fast shutter speed will result in a sharp photographic image being recorded. Using a sample-hold with its aperture time of tens of nanoseconds effectivly decreases the aperture time of the ADC by several orders of magnitude.

Sample-hold amplifiers are used with an ADC whenever the analog input signal's value may change by more than one half the least significant bit (LSB) of the ADC while a conversion is taking place. This criterion is easily checked by looking at the maximum value of the input signal's slew rate and multiplying this value by the aperture time. For a sinusoidal input with a maximum frequency f_m and maximum amplitude of V_m; the maximum slew rate is given by

$$SR_{max} = 2 * \pi * f_m * V_m. \qquad (2.2)$$

The maximum change of the input signal during the aperture time of the ADC is then

$$SR_{max} * t_{AP} = \Delta V. \qquad (2.3)$$

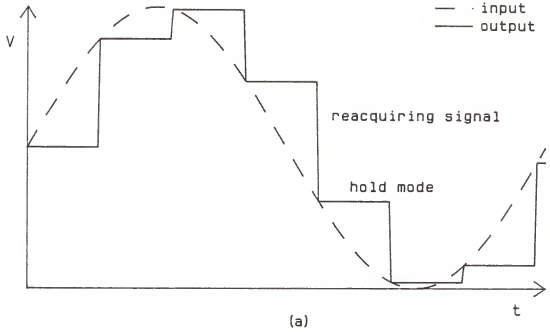
III. Sample-Hold Theory and Operation

This section of the report acquaints the user with the basic theory of sample-hold operation as well as with many of the practical deviations of sample-holds from these ideals. The ideal sample-hold is first described and then the characteristics of actual sample-holds compared with these. The error sources of pratical sample-holds are discussed in detail as are the noise sources in sample-hold amplifiers. The track-and-hold amplifier is then discussed and the use of low power track-and-hold amplifiers for band- and amplitude-limited systems is discussed.

Implementing the Sample-Hold.

The ideal sample-hold should be able to acquire any input signal with no error in an infinitesimally short period of time and then hold that value as a constant output for an infinitely long period of time. There are no devices today which can achieve this ideal state, although many configurations come close enough to be usable with good results. The main differences from the ideal sample-hold are finite acquisition times and hold mode voltage drifts. Figure 3.1 illustrates the contrast between an ideal sample-hold and a generalized output of a practical sample-hold.

The easiest way to hold an analog voltage is by storing energy and all sample-holds today contain energy storage elements, usually in the form of capacitors. The simplest sample-hold is in fact just a capacitor with a switch, as shown in Figure 3.2a. The capacitor by itself presents problems as a low impedance output from the capacitor will cause it to



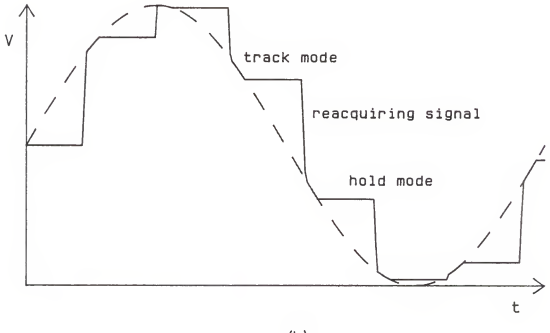


Figure 3.1. Comparison of (a) ideal and (b) practical sample-hold outputs.

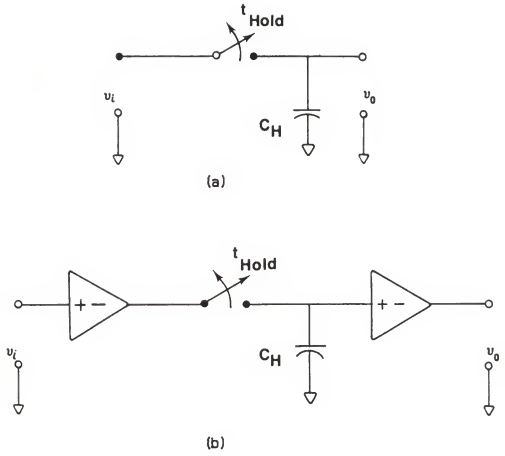


Figure 3.2. Basic sample-hold implementation methods: (a) switch and capacitor, (b) buffers added.

discharge very quickly when the switch is opened and a low impedance input is needed to the capacitor in order to charge the capacitor quickly. Figure 3.2b shows the general method of solving these problems by adding buffer amplifiers at the sample-hold input and output. The first buffer will provide the low impedance source needed by the capacitor for rapid charging and acquisition, while the output buffer presents a very high input impedance to the capacitor to minimize loading problems from following portions of the circuit.

In practice the buffers used to construct sample-hold amplifiers are usually operational amplifiers because these devices have high input and low output impedance and good current drive. The switches are usually some form of an FET switch which can be switched electronically and has an acceptably low "on" resistance. In order to give the sample-hold a short acquisition time operational amplifiers are used with high slew rates to enable the sample-hold's output to reacquire any possible change in the input signal which occurred during the hold mode. Using these high speed operational amplifiers will result in very useful and very power hungry sample-hold's which can operate with input frequencies of hundreds of kilohertz.

Figure 3.3 shows three of the most common sample-hold circuits. Each of the feedback configurations have unique advantages. The open-loop follower of Figure 3.3a has a fast acquisition time and small sample-to-hold mode transition glitches. In this configuration both operational amplifiers operate in a unity gain configuration. The first operational amplifier follows the input signal at all times and provides the

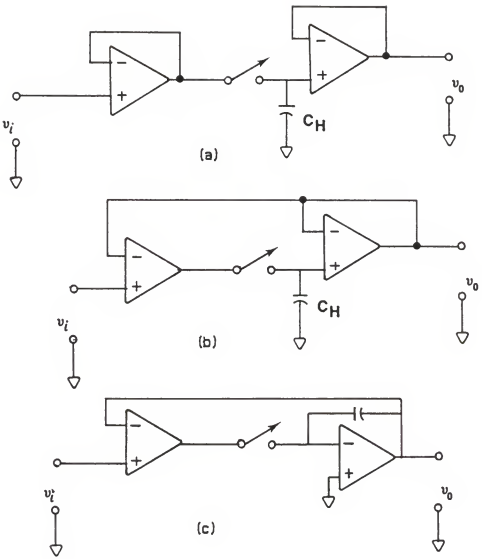


Figure 3.3. Common sample-hold circuits (a) open-loop follower, (b) closed-loop, (c) closed-loop integrator.

current needed to charge the capacitor during the sample mode. When a hold occurs, the switch is opened and the first operational amplifier will continue to track the input signal. The second operational amplifier buffers the capacitor from any output loading.

The closed loop sample-hold of Figure 3.3b has good a low frequency response. The first operational amplifier again operates as an input buffer and should have a high gain. This operational amplifier's current output will charge the hold capacitor, causing it to follow the input voltage. When the switch is opened the second operational amplifier again acts as a unity gain output buffer. The closed-loop integrating amplifier of Figure 3.3c is only one possible configuration of this type of sample-hold. The closed-loop integrating sample-hold is configured for noninverting unity gain operation as shown. The closed-loop integrating sample-hold can also be configured to have positive or negative gains other than one by adding a resistor to the feedback path and a second resistor between the positive input to the first operational amplifier and either ground or the input signal respectively.

Sample-Hold Error Sources

Although the configurations shown in Figure 3.3 provide good results, the sample-hold has many sources of error which cause its output to deviate from the input voltage at the time at which the hold mode was initiated. Many of the errors which will be discussed in greater detail later in this section are illustrated in Figure 3.4.

The Capacitor. The ideal sample-hold operates as an analog

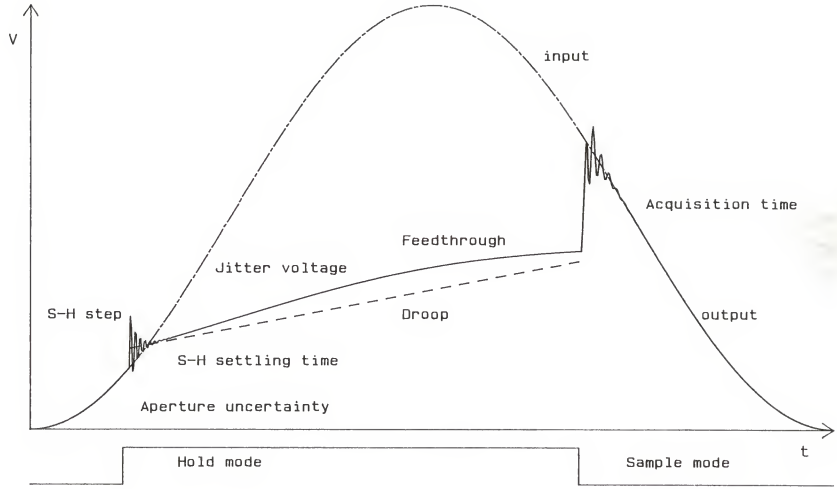


Figure 3.4. Practical sample-hold output waveform errors.

memory device caplable of "freezing" any input signal at any given instant in time. Actual sample-holds do this by storing energy. Capacitors are used as the energy storage elements since they are much better approximations of an ideal element than are available inductors. One of the key figures of merit for an energy storage element is its self-discharge time constant. For capacitors this figure is given by the product, R_cC, where R_c is the internal resistance of the capacitor. The product of R_cC for capacitors may be greater than 10E6 seconds, while the self-discharge time constant for inductors, given by L/R_i, may only be 10 seconds.

Other sources of sample-hold error which come from the hold capacitor are the hold capacitor's leakage current and any hold voltage error arising from the capacitor's dielectric absorption. The leakage current through the hold capacitor can contribute to the magnitude of the droop rate of the sample-hold. The capacitor's dielectric absorption can cause the hold capacitor's voltage to drift toward its previous value. This memory effect can be minimized by the proper selection of the type of dielectric used in the hold capacitor. Teflon capacitors have the lowest dielectic coeffecient and are usually specified for the hold capacitor. These factors and others which affect the selection of the hold capacitor are discussed in Appendix A.

The Switch. Sample-hold errors arising from the CMOS analog switch are primarily from the charge transfer and feedthrough. The charge transfer is the main cause of the hold step. The amount of charge transferred is dependent on the switch construction and the gate to drain voltage on the switch. This

error can be considered constant at any given voltage so that this error in the absolute voltage can be accounted for in system calibration. The magnitude of the charge transfer's component of the sample-to-hold offset voltage can be determined by

$$\Delta V = (\Delta Q / C) \qquad (3.1)$$

where ΔV is the magnitude of the voltage step, ΔQ is the amount of charge transferred, and C_H is the hold capacitor.

The easiest method of reducing the effects of the charge transfer is to use the largest hold capacitor possible which does not degrade any other sample-hold characteristics below acceptable levels. One way to make the charge transfer independent of the input voltage is to use one of the sample-hold configurations which have the switch output at virtual ground. This configuration will always have the same amount of charge transfer since the switch's gate to drain voltage step will be constant when the switch opens.

The feedthrough of the switch is the capacitive coupling of the switch's input and output by stray capacitance in the switch. The feedthrough isolation of the switch will indicate the amount of isolation the switch can achieve in the off state. The feedthrough isolation of a CMOS switch is normally greater than 70 dB.

The Operational Amplifier. The operational amplifiers used in constructing sample-hold amplifiers bring all of their inherent error sources to the sample-hold. The operational amplifier characteristics which are of primary concern to the sample-hold designer are: the input offset voltage and input

bias voltages, the input offset and input bias currents, the gain, the CMRR, and the PSRR.

The input offset voltage will cause an offset in the sample-hold's output. The input bias and offset currents are of concern because these currents are the main source of the hold mode's droop. For this reason operational amplifiers should be chosen with the lowest available specifications for these parameters. The gain is of interest to the designer because most of the circuits require a high gain in order to track the input with a high precision. The operational amplifier's CMRR also needs to be as high as possible so that output errors will not occur when large input voltages are encountered. The PSRR of the operational amplifier is an indication of its ability to reject noise from the power supply. If this value is not as large as possible the sample-hold output may contain unwanted noise from the power supply lines.

Timing Uncertainties. The timing uncertainties involved with the sample-to-hold transition are one of the largest sources of unpredictable errors in the sample-hold system. The two important timing quantities for this transition are the aperture delay time and the aperture delay jitter. The aperture delay time can be considered as a constant time delay between the hold command and the initiation of the hold mode. Since the aperture delay time can be thought of as a constant it will not cause any error in the overall function of the sample-hold because the aperture delay time can be taken care of by advancing the hold command by the same amount of time. In signal processing applications the aperture delay would result in a delta t being

added to the absolute time of each measurement point, which would have no affect on later processing methods.

The aperture delay jitter however, is an uncertainty in the point in time at which the hold mode originates. The magnitude of the aperture jitter is usually less than 100 nanoseconds, but even this small time can cause large errors when the input signals are of high frequency. Referring to equation 2.1, the magnitude of the output voltage uncertainty for a given input frequency and aperture delay jitter can be calculated. For a sample-hold with a 100 kilohertz 10 Vpp input and an aperture delay jitter of 10 nanoseconds the output voltage jitter would be:

$$(5)(2)(\pi)(100E3)(10E-9) = 3.14E-2$$

or 31.4 millivolts. This means that the hold mode voltage would be accurate to within plus or minus 31.4 millivolts of the input signal. This uncertainty limits the above sample-hold application to ADC systems of seven bits or less resolution. Since the aperture delay jitter is device dependent the user must take care in selecting a device which has an acceptable output error caused by the aperture delay time jitter. The resolution available from an ADC for a given aperture jitter and input frequency is shown in Figure 3.5 [2]. These values are independent of the input conversion range of the ADC since:

$$\Delta v = t_{APU} * dv/dt \tag{3.2}$$

where,

$$dv/dt_{max} = V_{max} * (2 * \pi * f) \tag{3.3}$$

and

$$\Delta v = 0.5 * V_{range} / 2^N. \tag{3.4}$$

Since V_{max} for a sinusoidal input should equal 1/2 V_{range} the

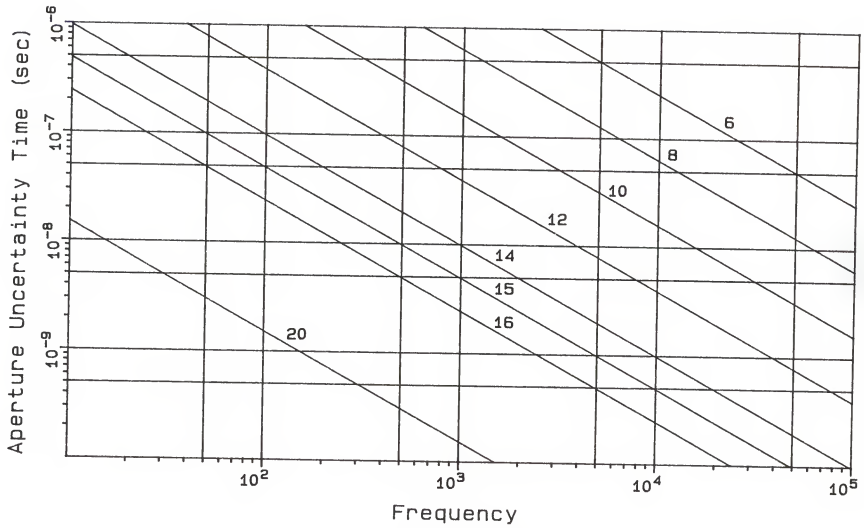


Figure 3.5. Sample-hold accuracy possible at various aperture uncertainties and input frequencies. Lines are 1/2 LSB error for indicated number of bits.

resolution of an ADC designed for sinusoidal inputs is not dependent on the conversion voltage range.

Sample-Hold Noise Sources

The noise contribution of the sample-hold amplifier to the output signal has three main sources: the operational amplifiers, the passive elements and power supply noise feedthrough.

Operational Amplifiers. The operational amplifiers in the sample-hold will contribute both voltage and current noise to the output signal. An operational amplifier's noise spectrum can be characterized by 1/f noise to a 1/f corner frequency and white noise above the 1/f corner frequency. The amplifiers noise contribution over a given bandwidth can then be calculated by [3]

$$N_{(fu-fl)}=N_0[f_0\ln(fu/fl)+(fu-fl)]^{1/2} \qquad (3.5)$$

where: $N_{(fu-fl)}$ is either voltage or current noise, N_0 is the white voltage or current noise density, and f_0 is the corner frequency of the 1/f and white noise components. Figure 3.6 illustrates a sample noise spectrum such as those which may be given in an operational amplifier data sheet. This figure is representative of both voltage and current noise, although the corner frequency for current noise is usually a decade higher than that for voltage noise.

Looking back at the sample-hold circuit configurations it can be seen that only the operational amplifiers used as output buffers will contribute noise to the hold mode of the sample-hold. Most of these output buffers operate in a unity gain configuration and therefore have a wide bandwidth. In this situation the noise output of the amplifier can be approximated very closely with a simplified version of equation 3.1

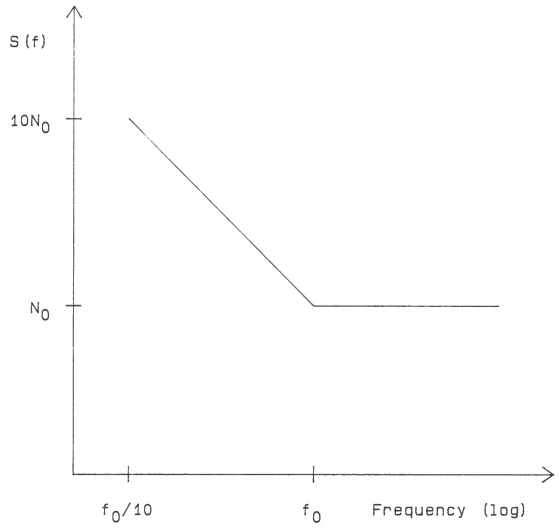


Figure 3.6. Sample operational amplifier noise spectrum.

$$N = N_0(\text{unity gain bandwidth})^{1/2} \quad (3.6)$$

The magnitude of the noise component added to the signal by the operatinoal amplifiers is usually less than 50 microvolts.

Passive Elements. The primary source of noise in the passive elements is the current noise output from the operational amplifier which is fed into any output filter and the thermal noise from any resistor in the output filter. The noise contribution from the noise current is [3]

$$V_{noise} = (\text{current noise} * \text{filter equivalent resistance}). \quad (3.7)$$

The noise from the the resistor would be given by[4]

$$(\text{Resistor Voltage Noise})^2 = 2kTR \quad (3.8)$$

where k is Boltzmann's constant (1.38 E-23 joule per Kelvin), and T is the absolute temperature (Kelvin). The total noise in the system is then given by the square root of the sum of the squares of the noise sources. From Equations 3.3 and 3.4 it can be seen that minimizing the equivalent resistances in the analog signal path will reduce the noise generated by the passive elements.

Noise Feedthrough from the Power Supply. The feedthrough of noise from the power supply lines is one source of noise that the designer can and must control. The proper filtering of the power supplies is essential in higher resolution systems since most analog IC's have power supply rejection ratio (PSRR) values that fall off at higher frequencies, especially on the negative power supply. The implementation section of this report deals with specific methods of power supply noise reduction and PSRR values for several operational amplifiers. One note of caution to the analog designer is to test any analog IC for its PSRR over frequency, since most data sheets give a PSRR value for nearly DC

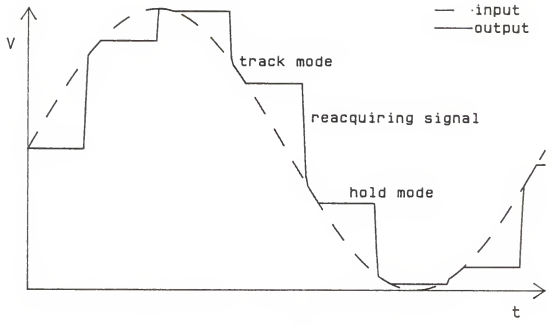
conditions. Ground line noise should also be avoided by use of proper ground connection techniques.

The Limited Slew Rate track-and-hold Amplifier

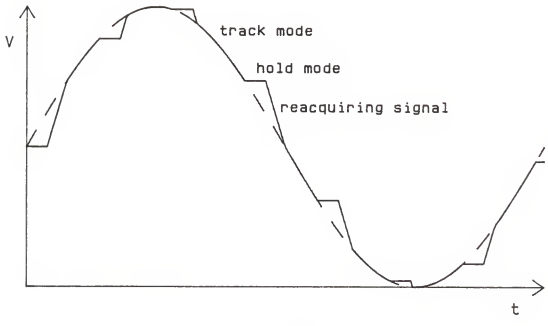
Sample-Hold amplifiers by definition should be able to acquire and hold their input signal in an infinitely short period of time. This capability requires them to have an infinite slew rate and zero acquisition time. (Acquisition time being the time required for the sample-hold to reacquire the input signal to a desired accuracy once the sample mode is initiated.) In order to approximate these requirements most sample-hold amplifiers available today use very high speed operational amplifiers with large current drive capabilities. These operational amplifiers have power requirements that make them prohibitive for use in many low power data acquisition systems that require sample-holds. In order to aleviate this problem it was decided to develope a track-and-hold amplifier that uses readily available low power operational amplifiers.

Track-and-Hold amplifiers differ from the ideal sample-hold amplifiers in that they do not instantly acquire and hold the input signal. Rather, track-and-holds have an extended sampling period which may give them a 90% or greater duty cycle in the sample mode. This difference between the idealized sample-hold and the track-and-hold amplifiers is illustrated in Figure 3.7.

Since track-and-hold amplifiers have a longer time period in which to acquire the input signal it was decided that the use of high slew rate operational amplifiers in sample-holds may not always be necessary. In fact, the problem of amplifier speed



(a)



(b)

Figure 3.7. Comparison of (a) sample-hold and (b) track-and-hold outputs.

becomes more one of the minimum slew rate of the operational amplifiers used in the track-and-hold. As an example consider an instrumentation system in which the input signal has been both frequency- and amplitude-limited. In such a system the maximum input slew rate can not exceed the slew rate of the largest magnitude highest frequency input. Since the input is magnitude-limited, adding additional frequency components to the input signal would at some point exceed the magnitude limit. Therefore the maximum slew rate of the input signal would again be given by Equation 2.1.

With a knowledge of the maximum input signal slew rate and the conversion time of the ADC to be used in given application, an idea of the slew rate required for the sample-hold to acquire the input signal can be derived. For an instrumentation system where the maximum input frequency is 100 Hz and the input amplitude is 10 V_{pp}, the maximum change in the input signal during a 1 msec analog to digital conversion would be less than:

$$(5*2*\pi*100 \text{ V/sec})*(1 \text{ msec})=3.141 \text{ volts.}$$

If the input signal was being sampled at a rate of 250 samples per second then a sample would be required every 4 msec. Since this example allows 1 msec for the analog to digital conversion, 3 msec are available for the sample-hold acquisition time. The sample-hold must be able to slew the 3.141 volts and any additional amount that the signal will changes if it is to acquire the input signal before the next hold mode.

A worse than worst case example of the slew rate required for the above signal would be if it was required to swing from either rail to the other during the 3 msec sample mode. In order

to do this the operational amplifiers used in the sample-hold must have a slew rate greater than 10V/3000 usec, or .0033 uV/usec. Today operational amplifiers are available that use microwatts of power and have slew rates of .005 uV/usec. This example shows the basis for the use of low power operational amplifiers in low frequency band- and amplitude-limited data acquisition systems. These low power sample-holds are actually used as track-and-holds and cannot be used as true sample-holds.

The low power track-and-hold developed in this paper cannot be used as a sample-hold because its acquisition time is most likely in milliseconds, rather than microseconds. This difference will limit the track-and-holds to very low input frequencies and sample rates of only a few kilo-hertz but, as long as their aperture times remain small, there should be no difference in their performance in these systems when compared to the higher speed sample-holds.

Another advantage of the track-and-hold over the sample-hold amplifier for instrumentation systems is that the effects of dielectric absorption can be reduced by staying the the sample mode as long as possible. Since this is the normal method of operation for track-and-holds, this source of measurement error can be reduced.

IV. Implementing a Low Power Track-and-Hold

This section of the report deals with the design and testing of a low power (less than five milliwatts per channel) track-and-hold amplifier. The track-and-hold amplifier had the following design requirements: lowest possible power consumption, accuracy and resolution suitable for use with a 15-bit ADC, and the ability to operate with an input signal with a maximum frequency of 50 hertz and a maximum amplitude of ± 5 volts at a sampling rate of 128 hertz.

To meet the given requirements of the sample-hold, it was seen that the available options were to either use a standard sample-hold amplifier in a power switched mode [5], or to design a track-and-hold amplifier around the programmable operational amplifiers which are available today. (Keep in mind that the difference between sample-holds and track-and-holds is primarily the duty cycle of the track, or sample, mode.) The second option was chosen because if successful, the track-and-hold method would provide a simpler implementation from a control standpoint.

Three different track-and-hold circuit configurations were built using the programmable operational amplifiers. These circuits were then tested using the procedures outlined in Appendix A. The first configuration to be discussed is the closed-loop follower, the second the closed-loop integrator, and the third the open-loop voltage follower. These circuits were constructed using programmable operational amplifiers and the results for each configuration are compared. The open-loop follower was also built using two different programmalble

operational amplifiers in order to compare their performance.

The operational amplifiers are said to be "programmable" because their power consumption can be selected by the choice of the set resistor, R_{set}. The choice of the value of R_{set} involves tradeoffs in lowering the operational amplifier's bandwidth and slew rate in exchange for less power consumption. The value for R_{set} is chosen with the aid of the curves and equations supplied by the manufacturer's data sheets [6].

As an example of the selection of R_{set} for the Precision Monolithics OP 22 operational amplifier so that its power consumption is less than one milliwatt use the following equation [6]

$$R_{set} = (V_{supply} - 2V_{BE}) / I_{set} \qquad (4.1)$$

where V_{supply} is the positive supply voltage and I_{set} is the desired set current obtained from the Supply Current vs Set Current curve. The supply current is chosen to give the desired power consumption. Using this method, the value of R_{set} needed for a power consumption of less than one milliwatt for the OP 22 operational amplifier is R_{set} greater than one megohm. In practice most of the circuits which were built and tested used R_{set} equal to two megohms for a nominal power consumption for the OP 22 of .53 milliwatts.

The Closed-Loop Track-and-Hold

The closed-loop track-and-hold is characterized by a good low frequency tracking of the input signal since it tends to act as a single amplifier stage when in the sample mode. This track-and-hold configuration is in widespread commercial use and was

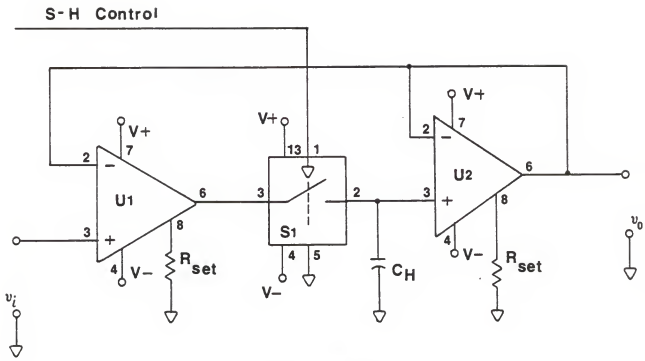
referenced in many sources; [2], [7], [8]. A closed loop track-and-hold circuit diagram is shown in Figure 4.1. When the circuit was constructed as shown in Figure 4.1 using either the Motorola MC 1776 or the PMI OP 22 pin compatible operational amplifiers the track-and-hold would oscillate at 10 to 15 kilohertz with an amplitude of 50 to 100 millivolts.

The linear system analysis package was then used to study the pole zero positions of this system. This system and those that follow in the report were simulated using the OP 22 operational amplifier's gain response to generate a two pole model of the operational amplifier. The system used to simulate the closed-loop track-and-hold which has the following open loop transfer equation

$$\frac{2.401E+19}{(jf - 3.5E4 \pm 6.06E4)(jf - 7E4)(jf - 7.957E3)(jf - 3.509E-2)} \quad (4.2)$$

Using these roots, the root locus plot of Figure 4.2 was generated. The root locus plot shows that a pair of roots for this system are complex conjugate pairs in the right half-plane. At unity gain the roots in the right half-plane are at 1.27E4±j4.57E4. This root location indicates exponentially increasing oscillation at 45.7 kilohertz, which is three to four times the observed constant amplitude oscillation. This difference probably comes from some inaccuracy in locating the poles of the operational amplifier.

Although some investigation was made into methods of stabilizing the closed-loop track-and-hold no satisfactory results were found. The literature [8] which documented this type of sample-hold stated that the first amplifier needed to be a



U1 = U2 = OP 22 or MC 1776
S1 = ¼ DG 309
R_{set} = 2.0 MΩ
C_H = 0.01 μf Teflon M
V+ = 7.5 V_{DC}
V- = -7.5 V_{DC}

Figure 4.1. Circuit diagram of the closed-loop track-and-hold.

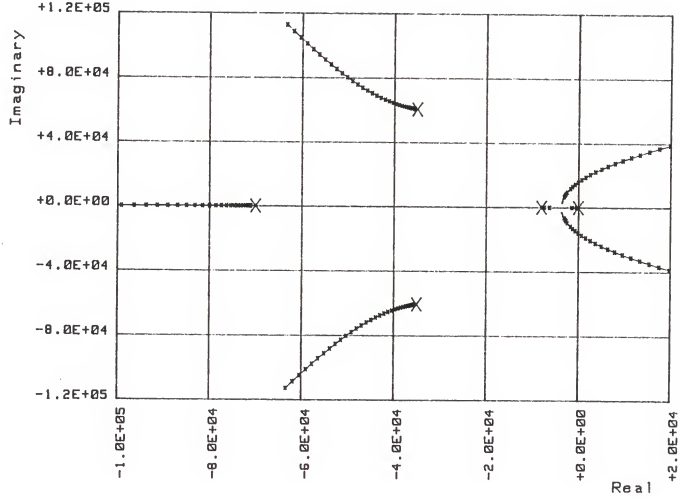


Figure 4.2. Root locus plot for the closed-loop track-and-hold.

high gain amplifier. If this amplifier had a large gain bandwidth product the location of the poles near the origin may be moved far enough apart to keep the roots in the left half-plane at unity gain. Implementing the higher gain amplifier would have greatly increased the power consumption of the overall system so this alternative was not attempted. Since this track-and-hold configuration proved to be oscillatory no further measurements were made on this system.

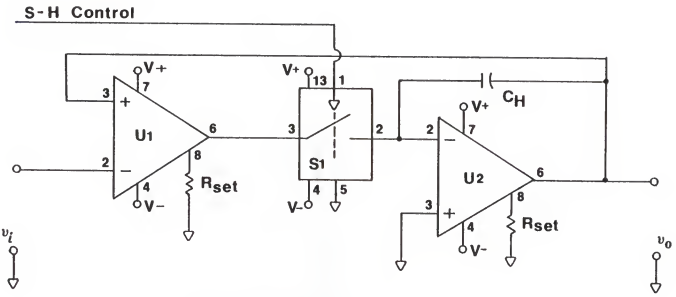
The Closed-loop Integrator Track-and-Hold

The closed-loop integrator configuration is characterized by good low frequency signal tracking and operation of the sample-hold control switch at virtual ground. Operating the switch at virtural ground will cause a constant sample-hold offset step and eliminate some of the feedthrough leakage currents to the hold capacitor, giving a better droop rate. The closed-loop integrator track-and-hold was constructed as shown in Figure 4.3 and then tested. This track-and-hold configuration also proved to be unstable. When sampling zero volt DC, the output of this track-and-hold would oscillate between its output rails at its maximum slew rate, both positive and negative.

The HP Linear systems analysis package was again used to examine the root locus plot of this system. The system used to simulate the closed-loop integrating track-and-hold had the following open loop transfer equation

$$\frac{2.729E18}{(jf - 7E4)^2(jf - 3.5E-2)(jf - 4.0E-3)} \qquad (4.3)$$

Figure 4.4 shows the root locus plot of this system. The roots of this equation at unity gain are: -7.55E4 ± j2.039E4 and



U1 = U2 = OP 22
S1 = ¼ DG 309
R_{set} = 2.0 MΩ
C_H = 0.01 μf Teflon
V+ = +7.5 V_{DC}
V- = -7.5 V_{DC}

Figure 4.3. Circuit diagram of the closed-loop integrator track-and-hold.

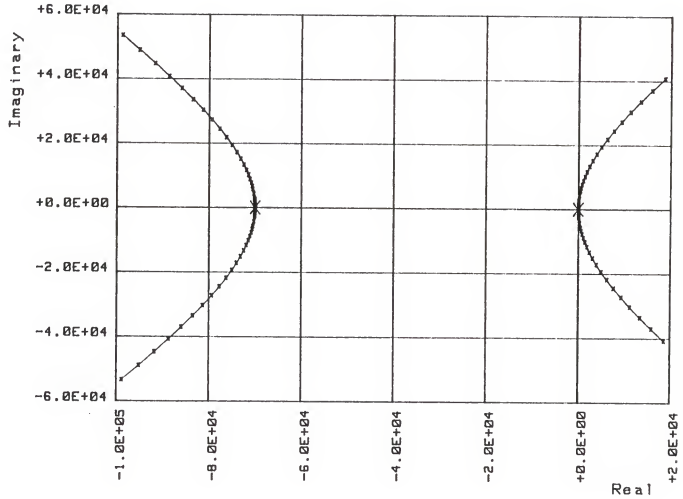


Figure 4.4. Root locus plot for the closed-loop integrator track-and-hold.

5.507E3 ± j2.0E4. Once again poles appear in the right half-plane at unity gain, indicating an unstable system.

The transconductance amplifier, a modification of the closed-loop integrating track-and-hold was found in the literature [2] and investigated. Figure 4.5 contains a schematic of this circuit. This configuration uses the feedback resistors to convert the feedback voltage into a current to charge the hold capacitor. This track-and-hold configuration was stable for certain values of R1 and R2 but the output range was clamped when the system was stabilized, see Table I.

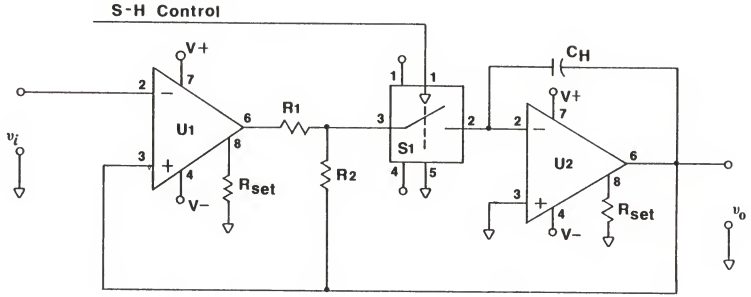
Table I

Maximum Output Amplitude of the Transconductance Amplifier

Resistance value in kohms R1	R2	Output Level in Volts peak to peak
7.5	0.1	0.2
7.5	1.0	2.25
7.5	2.2	5.0
7.5	3.0	6.6 with 46 mV oscillation at 11.9 kHz
7.5	4.7	10.5 with 100 mV oscillation at 10.9 kHz
10.0	2.2	3.7

The output of the transconductance track-and-hold was stable with a 10.5 volt peak to peak output when C_H was less than .002 microfarads.

The linear systems package was used to analyze the transconductance amplifier and with R1 equal to 7.5 kohms and R2 equal to 2.2 kohms the system had a complex conjugate pair of roots at 278 ± j3.6E3. This pair of roots would cause



$U_1 = U_2 = OP\ 22$
$S_1 = 1/4\ DG\ 309$
$R_{set} = 2m\Omega$
$C_H = 0.01\mu f$ Teflon
$V+ = 7.5\ V_{DC}$
$V- = -7.5\ V_{DC}$

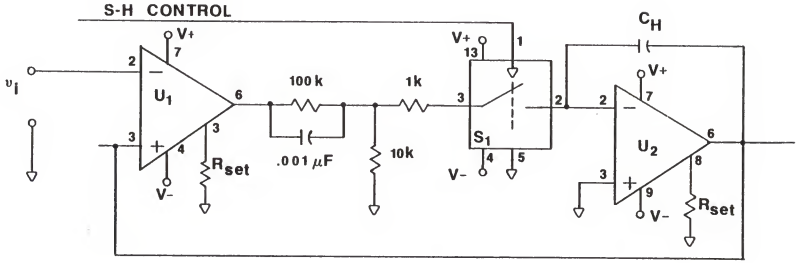
Figure 4.5. Circuit diagram of the transconductance track-and-hold.

oscillation at 3.6 kilohertz. Any error in modeling the circuit could mean that these roots are actually in the left half plane and the system may be very marginally stable as the experimental data shows.

Further methods of stabilizing the output of the integrating track-and-hold were investigated and the one which showed the best results was the addition of a lead-lag network. Figure 4.6 shows the altered integrating track-and-hold with the lead-lag network. Figure 4.7 and 4.8 show the root locus plot of this track-and-hold configuration while Figure 4.9 shows the magnitude and phase response of the closed-loop integrator with a lead-lag network.

The lead-lag network was able to provide unity gain stability to the track-and-hold but the complex conjugate pairs in the left half-plane near the imaginary axis indicate possible oscillations when step inputs are applied. The oscillations after step inputs may cause problems with track-and-hold operation because the device is subject to equivalent step inputs whenever it is switched from the hold to the sample mode. Having large or lightly damped oscillations can severely increase the acquisition time.

When this circuit was built and tested in the lab the circuit did show large spikes and oscillations after the initiation of the sample mode. The oscillations took up to four milliseconds to dampen out and would have increased the sample-hold's acquisition time to at least this same amount. Figure 4.10 shows a sample output of the circuit while the input signal was grounded. This track-and-hold was put through several tests



$U_1 = U_2 =$ OP 22
$S_1 =$ ¼ DG 309
$R_{set} = 2\,M\Omega$
$C_H = 0.01\ \mu f$ Teflon
$V_+ = 7.5\ V_{DC}$
$V_- = -7.5\ V_{DC}$

Figure 4.6. Circuit diagram of closed-loop integrator track-and-hold with lead-lag network.

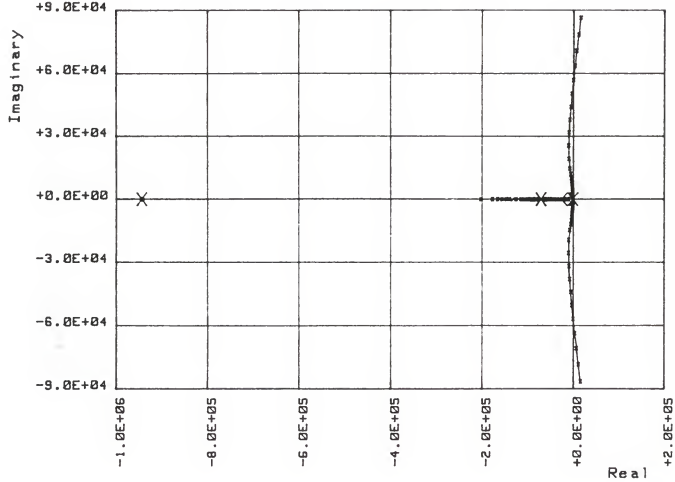


Figure 4.7. Overall root locus plot for the closed-loop integrator track-and-hold with lead-lag network.

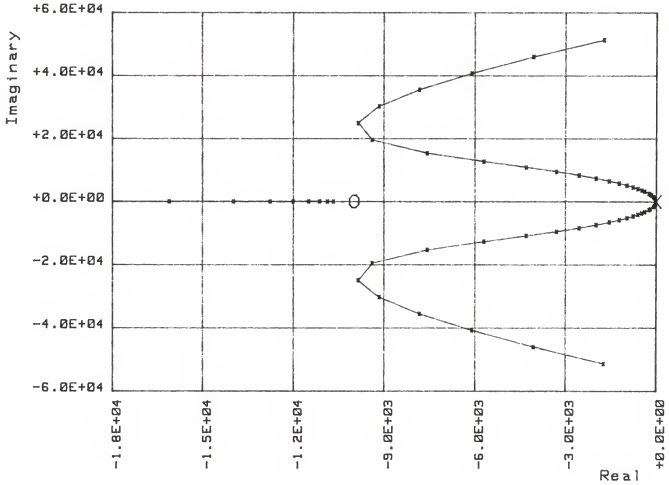


Figure 4.8. Expanded root locus plot showing the effect of the lead-lag network near the origin.

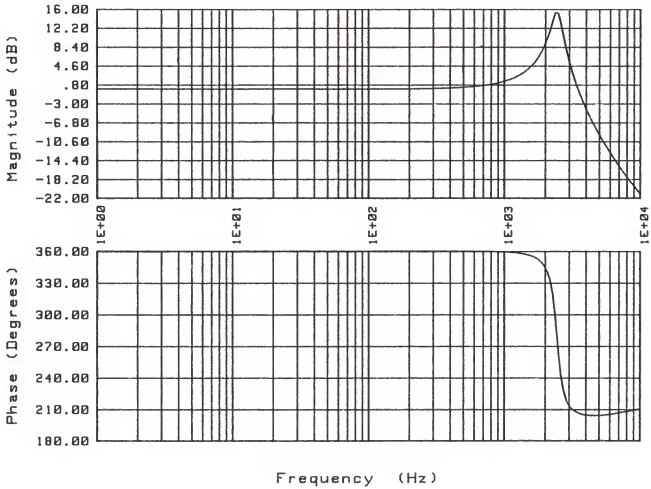


Figure 4.9. Magnitude and phase response of the closed-loop integrator with lead-lag network.

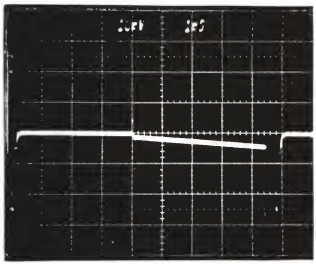


Figure 4.10. Sample output of the closed-loop integrator track-and-hold with input grounded and 110 hertz sample-hold signal.

This figure shows the long acquisition time for the closed-loop integrator track-and-hold with lead-lag network. The figure shows from the left the sample mode at ground, the sample-hold step, droop and acquisition period.

and the results are given below in Table II.

Table II

Performance Table for the Closed-Loop Integrator

Parameter	OP 22	Units
V_{offset}	0.7	mV
$V_{S-H\ step}$	-4.0	mV
Droop Rate	-0.8	uV/us
Slew Rate	0.005	V/us
Hold Mode Noise	150	uV pp
Acquisition Time	4.0	msec
Aperture Delay Time	7.0	usec
Aperture Delay Jitter	< 60	nsec
Maximum Trackable Frequency	200	Hz
Maximum Sample Rate*	200	sps
Power Dissipation	1.2	mwatts

* Maximum sample rate assumes 500 microsecond conversion time and 400 microsecond sample period.

The Open-loop Follower Track-and-Hold

The open-loop follower track-and-hold is usually used where fast acquisition times are needed. This type of track-and-hold can acquire the input signal quickly because the first operational amplifier is following the input signal during the hold mode. Then, when the sample mode is begun, the first operational amplifier should quickly drive the hold capacitor to the input voltage level. In the low power track-and-hold circuit the fast acquisition times are not important, but the circuit was built because it is one of the simplest track-and-hold designs.

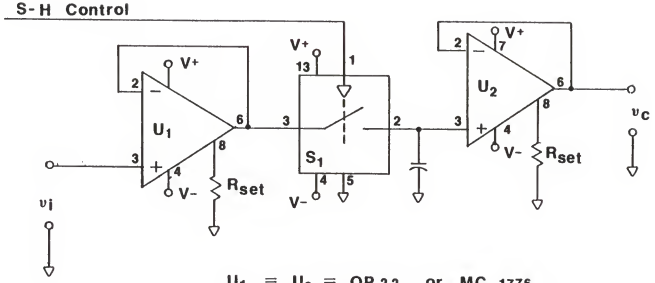
A circuit diagram for the open-loop follower is shown in Figure 4.11. The circuit was tested with both the Motorola MC1776 and the Precision Monolithics Inc. (PMI) OP 22 programmable operational amplifiers. The switch used in this test circuit was the Siliconix DG309. The Siliconix DG309 quad analog switch was used in all of the track-and-holds constructed because of its low power consumption and gate to drain capacitance. When tested the DG309 had only one third the gate to drain capacitance of the similar DG308, which resulted in a smaller sample-hold offset when the DG309 was used.

The HP Linear Systems Analysis package was used to predict the stability and performance of the open-loop follower track-and-hold. At unity gain this configuration had roots at -3.498E4±j6.068E4, -3.502±6.056E4, and -7.957E4. These roots indicate that the system should be relatively stable. Figure 4.12 contains the magnitude and phase response for the open-loop follower track-and-hold as calculated using the HP Linear Systems Analysis package.

While testing these circuits it was noticed that the hold mode voltage had a tendency to follow the input voltage. From the DG309's data sheet it was found that the off isolation of these switches was typically 78 dB. With 78 dB of isolation, the size of the voltage feedthrough, V_{ft}, in the hold mode would be given by

$$V_{ft} = (V_{in} - V_{Hold}) * 10^{(-78 /20)} \qquad (4.4)$$

With V_{in} equal to five volts and V_{Hold} equal to minus five volts the feedthrough voltage would be about 1.26 millivolts. This



$U_1 = U_2 =$ OP 22 or MC 1776
$S_1 =$ ¼ DG 309
$R_{set} =$ 2 MΩ
$C_H =$ 0.01 μf Teflon
$V^+ =$ 7.5 V_{DC}
$V^- =$ -7.5 V_{DC}

Figure 4.11. Circuit diagram of the open-loop follower track-and-hold.

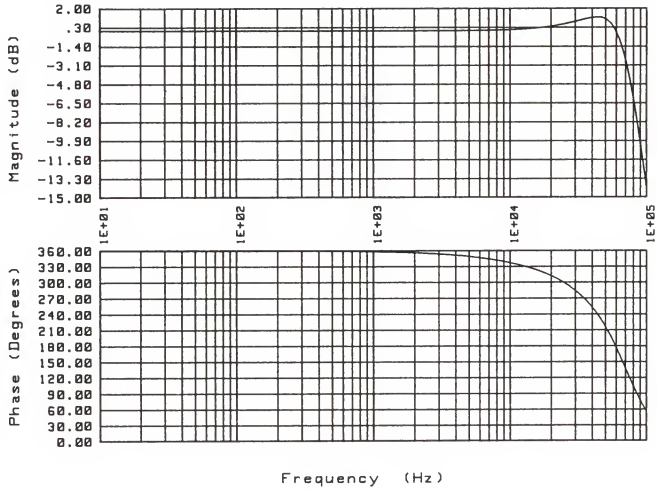


Figure 4.12. Magnitude and phase response of the open-loop follower track-and-hold.

magnitude of feedthrough would cause an error four times the size of the LSB of the 15-bit ADC for which this track-and-hold was designed. The 1.26 millivolts of feedthrough mentioned above would result from the input voltage varying by 10 volts during a hold mode. This system's input signal would have a maximum voltage variation of 1.56 volts during one twentieth of a cycle during which the track-and-hold is in the hold mode. (This figure assumes the maximum signal change centered about the zero crossing with a 10 Vpp input signal.) Using this worst case value to calculate the feedthrough voltage gives a maximum feedthrough in the hold mode of 196 microvolts, or about two thirds of an LSB. Since this value for the feedthrough can cause just over one-half LSB of error in the hold voltage the feedthrough isolation was checked experimentally.

In testing this system's voltage feedthrough, the feedthrough isolation for a single DG 309 switch was measured at 70 dB. With this off isolation, the voltage feedthrough becomes 490 microvolts, which is more than one and one-half LSB. In order to improve the feedthrough isolation it was decided to operate two of the switches in series. Operating the switches in series should provide more than 150 dB of isolation, or a maximum feedthrough voltage of 316 nanovolts. This circuit modification would be added to any sample-hold or track-and-hold built for operation with the 15-bit ADC. When tested this new switch configuration provided no detectable voltage feedthrough in the hold mode. Table III contains the parameters of the open-loop follower.

Table III

Performance Table for the Open-Loop Follower

Parameter	MC1776	OP 22	Units
V_{offset}	3200	-40	uV
$V_{S-H\ step}$	see Figure 4.13 (a).		
Droop Rate	-.43	0.8	uV/us
Slew Rate	0.08	0.02	V/us
Hold Mode Noise	400	220	uV pp
Acquisition Time	0.1	0.4	msec
Sample-hold settling time	100	100	usec
Aperture Delay Time	2.5	6.0	usec
Aperture Delay Jitter	< 60	< 60	nsec
Maximum Trackable Frequency	2000	300	Hz
Maximum Sample Rate*	1000	700	sps
Linearity	see Figure 4.13 (b).		
Power Dissipation	1.20	1.20	mwatts

* Maximum sample rate assumes 500 microsecond conversion time and 400 microsecond sample period.

The PSRR as a function of frequency for both the OP 22 and the MC 1776 operational amplifiers is shown in Figure 4.14. Figure 4.14 illustrates the frequency dependence of the PSRR, showing a 20 dB per decade decay. The noise signal applied to the positive supply was severely distorted at the output at frequencies above 20 kilohertz. In the lower frequency ranges where the experimental data shows a flat line the PSRR actually should continue to follow the 20 dB per decade slope. The experimental data do not show this because the HP 3478A

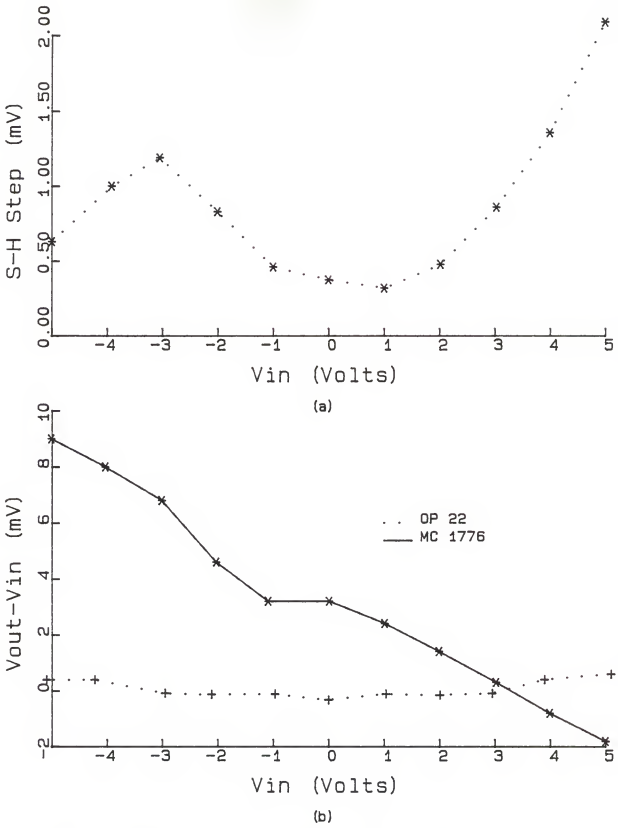


Figure 4.13. Open-loop follower parameters. (a) Voltage dependent sample-hold offset. (b) Linearity.

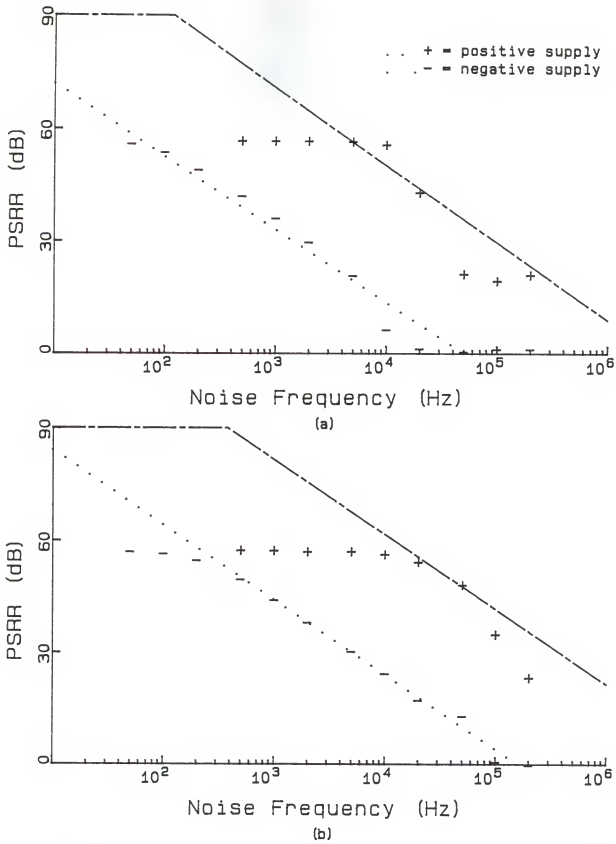


Figure 4.14. PSRR vs. Frequency for (a) OP 22 and (b) MC 1776. Dashed lines are the expected value.

multimeter displayed the rms value of the operational amplifier's noise output as well as any power supply noise feedthrough. This figure shows the importance of isolating the track-and-hold from power supply noise since the PSRR is 0 dB at frequencies as low as 1E5 hertz for the negative supply.

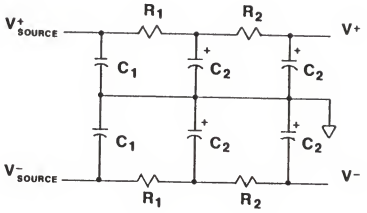
The power supply isolation network shown in Figure 4.15 will reduce the effects of power supply noise on the track-and-hold. This isolation network has two poles of isolation and the ceramic and tantalum capacitors have complementary frequency ranges in order to reduce both high frequency spikes and lower frequency variations. In practice this isolation network adds poles at 157 hertz and 15.9 kilohertz. The low frequency pole should give the track-and-hold the equivalent of 55 dB of PSRR over all frequencies on the negative and 70 dB on the positive supply.

Reducing Track-and-Hold Output Noise

Each of the track-and-hold configurations investigated had output noise amplitudes of greater than one-half the LSB of the 15 bit ADC. In order to reduce the output noise a low pass RC filter was added to the track-and-holds output. Filters with 3 dB points of less than 25 kilohertz gave good results.

The addition of the output filters will increase the hold mode settling times because the filter output will lag behind the voltage on the hold capacitor because of the phase shift of the low pass filter. The output filter would then take some time to acquire the hold mode voltage to within 100 microvolts. The following calculations were used to determine the worst case settling time of a low pass RC filter with a RC = 1 E-5.

Determining the amount of phase lag, phi, which is given by



$R_1 = 1\ \Omega$
$R_2 = 100\ \Omega$
$C_1 = .1\ \mu F$ Ceramic
$C_2 = 10.0\ \mu F$ Tantalum

Figure 4.15. Power supply isolation network.

$$\text{phi} = -\tan^{-1}(2*\pi*f*RC) \qquad (4.5)$$

For a frequency of 50 hertz phi is -0.17 degrees. The maximum voltage lag caused by this phase shift would then be at a zero crossing and its magnitude would be

$$V_{lag} = 5\ V * \sin(0.17) = 15.7\ mV \qquad (4.6)$$

The time required for the RC filters output to fall to within 50 microvolts of the 15.7 millivolt difference is then given by

$$t = -(\ln(50\ E\text{-}6 / 15.7\ E\text{-}3) * 1\ E\text{-}5) = 57.5\ usec \qquad (4.7)$$

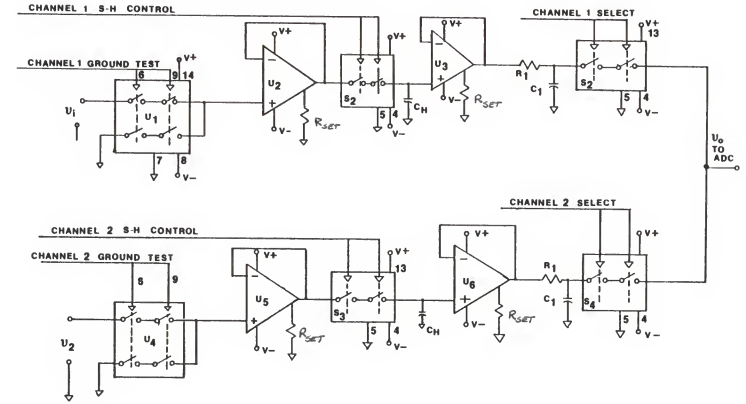
This 57.5 microsecond decay time must be included in the sample-hold settling time.

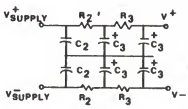
The Complete Two Channel System

The design requirements for the low power system included dual channel capability. Figure 4.16 shows the additional circuitry needed to implement the dual channel multiplexing and ground sampling. In this system the analog switches are again used with two in series to provide less than one-half LSB of feedthrough. The pin connections for the switches are not shown in the diagram because these can be varied as needed by the board layout. The one rule to remember when connecting the analog switches is to always have the input to the source (S input) of the switch in order to reduce spiking.

The DG 307 switches used in the circuit should use at most 0.15 milliwatts per package. The DG 309 should consume less than 0.1 milliwatts per package at the sample sample rates of less than one kilohertz. This brings the total power consumption of the two channel system to about 2.9 milliwatts with the OP 22 based track-and-holds or the MC1776 based track-and-holds.

The power consumption of one-half of the OP 22 based system





$U_1 = U_4 = DG\ 307$

$U_2 = U_3 = U_5 = U_6 = OP\ 22\ EZ$

$S_1 = S_2 = S_3 = S_4 = \frac{1}{2}\ DG\ 309$

$R_{SET} = 2\ M\Omega$

$R_1 = 10\ k\Omega$

$R_2 = 1\ \Omega$

$R_3 = 100\ \Omega$

$C_H = 0.01\ \mu F$ TEFLON

$C_1 = 0.001\ \mu F$ CERAMIC

$C_2 = 0.1\ \mu F$ CERAMIC

$C_3 = 10.0\ \mu F$ TANTULUM

Figure 4.16. Two channel track-and-hold and multiplexor.

was measured using the power measurement system developed by Charles Ragsdale [9]. These tests were performed with the track-and-hold channel operating at 130 hertz sampling rate with a 10 Vpp 50 hertz input. The results indicated that the single channel consumed 1.64 milliwatts of power, or 3.28 milliwatts for both channels combined. The measured power consumption was within 13% of the predicted value. The supply currents for both the MC 1776 and the OP 22 operational amplifiers have positive temperature coefficients. The variation in either operational amplifier's power consumption should be 0.3 milliwatts from -50 to 120 degrees Celsius.

Summary of Implementation Results

The data collected on the operation of the low slew rate track-and-holds shows that they can be used in place of higher power sample-holds with no distinguishable difference in applications requiring low sample rates.

The slew rate-limited track-and-hold design which seems to give the best results is the open-loop voltage follower. This configuration has advantages in its sampling rate that would make it useful in more applications. The open-loop voltage follower does have a low pass filter characteristic which must be considered. This filter characteristic will cause phase shifts in the sample data output and will attenuate frequencies of greater than 350 hertz by more than 1E-3%. The open-loop voltage follower also has the problem of the input amplitude dependent sample-hold step voltage. Using the closed-loop integrator would eliminate the input dependent sample-hold offset, but this track-and-hold's long acquisition times would limit the maximum input

frequency to less than 100 hertz.

The OP 22 operational amplifier provides the best results with its low offset voltage and high gain and CMRR. This operational amplifier should be used as the basis for any low power system where operation near the voltage rail is not needed. The bipolar input stage of the OP 22 will results in little variation of the input bias currents with temperature. This characteristic will lessen the variation of the droop rate with temperature. The DG 309 switch proved to have smaller charge transfer than its inverse logic twin the DG 308. The DG 309 should therefore be used in the low power track-and-hold configuration.

V. Conclusions

The results of the research into the use of low power operational amplifiers in track-and-hold amplifiers indicate that their use will provide performance suitable for use in 15-bit ADC systems as long as the limiting input signal amplitude and frequency constraints are followed. It is the recommendation of the author that the open-loop voltage follower type of track-and-hold be used since it combines both simplicity of design and stable performance. In using the open-loop voltage follower track-and-hold the following signal processing must take into account the low pass filter characteristic of the track-and-hold.

A complete two channel system with ground test and multiplexing capability is shown in Figure 4.16. This two channel system is being incorporated into the 15-bit digitizer developed for Sandia National Laboratory at Kansas State University. The low power track-and-hold system has equal or better performance at low frequencies than most sample-holds requiring ten or more times the power. This design will also operate at higher sample rates without the large increase in power consumption a switched supply system would have.

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GLOSSARY

ADC. ADC refers to Analog to Digital Convertor which is a device which gives a digital representation for the value of an analog or continuous valued expression at various succeeding points in time.

Acquisition Time. Acquisition time is the time required for the sample-hold's output voltage to acquire the input voltage to within some given error band after the sample mode is initiated. In most cases this value is given for acquiring a DC level.

Aperture Time. Aperture time is the time during the sample-hold switch opening over which the input signal is integrated. This time is equivalent to the sample pulse width.

Aperture Delay Time. Aperture delay time is the time required for the sample-hold to initiate the hold mode once the hold command is given. This time may be either positive or negative in practice, as the effective hold point can occur before the hold command is given.

Aperture Delay Time Jitter or Aperture Delay Jitter or Aperture Uncertainty. These terms all refer to any uncertainty in the aperture time. Any uncertainty in the aperture time can result in a hold voltage error proportional to the product of the signal's slew rate and the magnitude of the aperture jitter. The aperture delay jitter can also include in variation in the time it takes for the switch to open.

Common Mode Rejection Ratio (CMRR). The common mode rejection ratio of a differential amplifier is the ratio of any output voltage (referred to the input) caused by a common input voltage

to the common input voltage level.

Charge Transfer. Charge transfer is the transfer of charge via stray capacitance to the hold capacitor, C_H, from the switch when switching to the hold mode. The charge transfer is the primary source of the sample-to-hold offset. The size of the voltage error caused by the charge transfer is given by: $V=Q_{transfer}/C_H$.

Dielectric Absorption. Dielectric absorption refers to a capacitor dielectric's ability to "remember" previously applied voltage levels and then attempt to return to those levels if the capacitor is allowed to float with an open circuit.

Droop Rate. Droop rate is the rate of change in the sample-hold's output voltage during the hold mode. The slope of the hold voltage (dV/dt) may be either positive or negative, depending on the device tested. The droop is caused by the leakage current through the switch and bias and offset currents from the op amps used.

Feedthrough (Attenuation Ratio). Feedthrough is the amount of the input signal which appears at the sample-hold output during the hold mode. This value is usually given in dB and is a result of stray capacitance coupling the input and C_H, mostly through the open switch.

Hold Mode Settling Time. Hold mode settling time is the time after the sample-to-hold transition for all transients to decay to within some specified error band.

Hold Step or Sample-to-Hold Offset or Pedestal Error. Hold step is the magnitude of voltage step which occurs at the sample-to-hold transition.

Power Supply Rejection Ratio (PSRR). Power supply rejection

ratio is the ratio of the amount of a given power supply disturbance which appears at the devices output to the magnitude of the disturbance, usually given in dB. PSRR is largest at DC and decreases with frequency. Most manufacturers data sheets give a PSRR value without stating the frequency at which the data was taken.

Sample-Hold Amplifier. A sample-hold amplifier is an analog voltage memory device which is used to reduce the aperture time of an analog to digital convertor, or as a filter. Sample-hold is often used interchangeably with track-and-hold.

Slew Rate. Slew rate is the maximum rate of change in a voltage waveform. For most devices the slew rate would be the maximum rate of change in the output voltage can achieve.

Track-and-Hold Amplifier. A track-and-hold amplifier is an analog voltage memory device used to reduce the aperture time of an analog to digital conversion system. The track-and-hold varies from the sample-hold in the much higher duty cycle of its track or sample mode.

Appendix A.

Test Procedures for Evaluating Track-and-Hold Amplifiers

The tests performed to evaluate the track-and-hold operation were of two basic types. First, static tests were performed with the device under test having a DC input voltage. The second set of tests were dynamic and the track-and-hold was exercised with an sinusoidal input. These two sets of tests should give a good characterization of the track-and-hold's performance.

The Static Tests

When the circuit was constructed static tests were first performed. These tests included measuring the sample-hold offset, the droop rate, the input offset voltage, the hold mode output noise, a minimum sample-hold settling time and the output linearity of the track-and-hold. These tests were conducted with a ± 7.5 volt power supply using the test system shown in Figure A.1. The power supply rejection ratio tests will also be described in this section as they were done with the track-and-hold input at ground.

The test procedure for the sample-hold offset and the droop rate was to ground the track-and-hold input and then apply a square wave at several hundred hertz to the sample-hold control signal. The output of the track-and-hold was then monitored on the Tek 5441 storage oscilloscope. Figure A.2 is a sample output of one of these tests for the open-loop voltage follower constructed using the OP-22 operational amplifiers. This figure shows how the droop rate, the hold mode output noise, and the sample-hold offset could be easily measured. An minimum value of

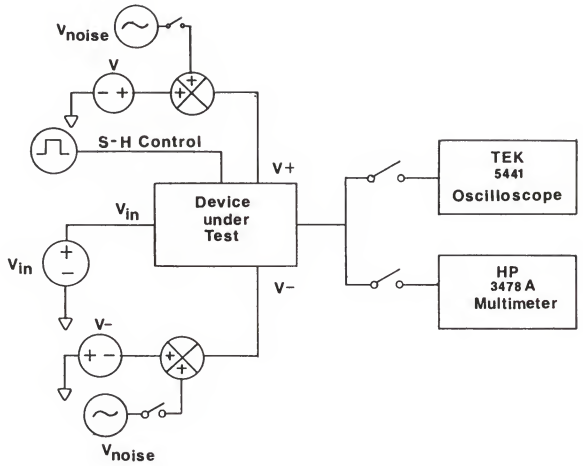


Figure A.1. Sample-hold static test system.

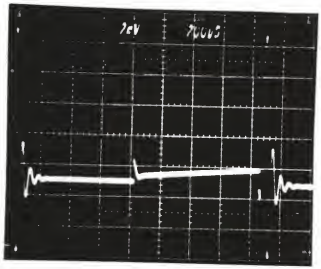


Figure A.2. Sample output of the static test system.

This figure shows the output of an open-loop follower track-and-hold using the OP 22 operational amplifier. The vertical axis is two millivolts per division and the horizontal axis is 200 microseconds per division. From the left the trace shows: oscillations during the acquisition time, flat ground tracking, sample-hold step, droop, and the the oscillations of a second acquisition period.

the sample-hold settling time is also easily determined by the time required for the hold mode output to settle to within 100 microvolts of its final value.

An idea of the track-and-hold's acquisition time could also be obtained by increasing the sampling rate until the hold mode voltage begins to vary. The variation in the hold mode voltage from ground would begin when the next hold period was being initiated before the track-and-hold was able to reacquire the input signal during the track period. The track period would then be the minimum possible value for the acquisition time.

Testing the linearity of the track-and-hold was done by applying a DC voltage to the track-and-hold's input and then measuring the output of the track-and-hold with with the HP 3478A multimeter. Data were then taken with the input DC voltage at various levels throughout the input range. The linearity is a function of the operational amplifier's CMRR.

The power supply rejection ratio tests were conducted on the track-and-hold with only a single 0.1 microfarad ceramic capacitor as power supply filter. The test procedure was to ground the track-and-hold's input and configure the device for a continuous tracking mode. A one volt peak to peak sine wave was then superimposed on one of the power supply voltages and the magnitude of the superimposed sinusoid was measured at the track-and-hold's output. The PSRR is then the ratio in dB of the output sinusoid amplitude to its input amplitude (usually the PSRR is expressed as a positive number.) This procedure was then repeated at frequencies of interest.

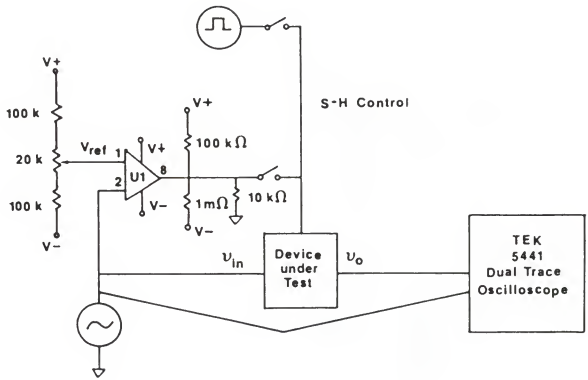
The Dynamic Tests

The dynamic tests performed on the track-and-hold amplifier were harder to perform in a qualitative fashion than the static tests. The primary instrument used to evaluate these tests was again the Tek 5441 storage oscilloscope. This scope was used because it had a resolution down to 10 microvolts per centimeter as well as storage and differential input capabilities. One drawback of the Tek 5441 was its one megahertz bandwidth which restricted the observation of many of the fast transitions in the track-and-hold.

The dynamic tests allowed the evaluation of the track-and-holds ability to track and acquire sinusoidal signals. These tests also provided the data for determining the maximum input frequency, the worst case acquisition time, the hold mode settling time, voltage feedthrough, the aperture delay, and the aperture delay jitter. The basic test system is shown in Figure A.3.

The first test was to apply a low frequency sine wave with the track-and-hold amplifier in a continuous tracking mode. While the input and output signals were monitored on the dual trace oscilloscope the input sinusoid was adjusted to the maximum allowable input amplitude. The input frequency was then slowly increased until the output began to deviate from the input signal. A second method of performing this test is to apply the input and output signals to the differential oscilloscope inputs. Then the difference between the input and output voltages can be readily observed down to 10's of microvolts.

Once the maximum input tracking frequency had been



U1 = 1/4 PM 339 Comparator

Figure A.3. Sample-hold dynamic test system.

determined the sample-hold control signal was connected to the square wave input. With the oscilloscope again in the differential ,but triggered from the sample-hold signal, mode and the input frequency a low frequency maximal amplitude sinusoid, it is possible to determine the acquisition time of the track-and-hold. Although the oscilloscope's display may be somewhat hard to understand keeping in mind that when the display shows a trace at ground that the input and output voltages are the same, or the input has been reacquired (see Figure A.4) The maximum time for the output to reacquire the input was then recorded. This method may not be usable for all systems, such as the open-loop voltage follower, because these systems have some phase shift on the output which will cause the differential input/output voltage to be larger than zero even after the track-and-hold has acquired the input. For these systems the acquistion time was measured using the same tests procedures except for grounding the input scope lead. The acquisition time is then observed from the scope trace.

The feedthrough isolation was measured using the dynamic test circuit of Figure A.4 with the comparator used to trigger the hold mode when the input voltage was at Vref. This configuration made it possible to initiate a hold mode at the zero crossing. Since the droop of the hold voltage was essentially linear and the feedthrough at either end of the hold mode should be nearly zero, any other deviation in the hold voltage would be attributable to switch feedthrough. The magnitude of the feedthrough voltage was then measured by determining the deviation of the scope trace from a line

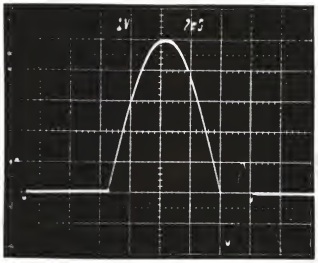


Figure A.4. Sample output of the dynamic test system.

This figure shows a sample output trace of the dynamic tests performed on the closed-loop integrator track-and-hold. The scope was in the differential input mode with 1 volt per division vertical scaling and 2 milliseconds per division on the horizontal scale. The ground trace on the left occurs when the input and output are at the same voltage, or the track-and-hold has acquired the input signal. The half sinusoid is the hold mode and the two millisecond gap to its right is the acquisition time for this case.

connecting the beginning and end of the hold voltage. The ratio in dB of the maximum feedthrough voltage to the maximum input then gave the feedthrough isolation of the switch.

In order to look at the aperture delay time and the aperture delay jitter it was decided to look at the voltage errors caused by these time errors rather than the time errors themselves. In order to look at these uncertainties a method of triggering the hold mode at the same point on the input signal waveform was needed. The triggering method which gave the best results was the simple comparator with an adjustable voltage reference. In use, this system caused the hold mode to be initiated at the time at which the input signal crossed the reference voltage plus the propogation time of the comparator. Although this system gave very good results when the input signal was filtered the values obtained will not be exact numbers for normal track-and-hold operation because it was necessary to operate the track-and-hold switch from a single supply (by connecting the ground connection of the DG 309 to V-). Operating the switch in this fashion will slightly lengthen the switch opening times but should have no effect on the aperture delay jitter.

Once the circuit was ready to be triggered by the comparator, a maximum amplitude and frequency input signal was again applied. The comparator voltage reference (V_{ref}) was then adjusted so that the hold mode was initiated near the zero crossing. The magnitude of the voltage error caused by the aperture delay jitter was then easily observed with the oscilloscope set to a high resolution. An idea of the magnitude of the voltage error was readily obtained by placing the

oscilloscope in its storage mode for several seconds. Calculating the magnitude of the aperture delay jitter was then a simple application of equation 2.1. Knowing the magnitude of the voltage varition, Δv, and the derivative of the input signal the aperture delay jitter, t_{ADJ}, was calculated from:

$$t_{ADJ} = \Delta v \; / \; (dv/dt) \qquad (A.1).$$

The method for measuring the aperture delay time required the use of the comparator triggering circuit. To measure the aperture delay time the voltage reference was adjusted so that the hold was initiated just at zero volts. The value of V_{ref}; the track-and-hold offset voltage, V_{ofs}; and the sample-hold offet, V_{sh}, were then used to calculate the aperture delay time, t_{AD}, as shown in equation A.2:

$$t_{AD} = (-V_{ref} - V_{ofs} - V_{sh}) \; / \; (dv/dt) \qquad (A.2).$$

Equation A.2 was developed on the assumption that the track-and-hold would slew by the amount of V_{ref} less any offset voltages during the aperture delay time.

Appendix B.

Capacitor Characteristics for Sample-Holds

This appendix details those capacitor characteristics that need to be considered in the selection of the hold capacitor used in any sample-hold. The main capacitor characteristics which must be considered are the insulation resistance, the temperature stability, and the dielectric absorption. Table B1, taken from an article by Walter G. Jung and Richard Marsh, Selection of Capacitors for Optimum Performance - Part 2, Picking Capacitors, Audio, March 1980, p. 56, shows an overall comparison of the qualities of the various capacitor dielectrics available today.

The insulation resistance is inversly proportional to the leakage current through the capacitor. The leakage resistance is usually specified in units of megaohms per microfarad. Since any current flowing through the hold capacitor will affect the droop rate of the sample-hold, maximizing the insulation resistance will reduce the droop voltage caused by the capacitor leakage current. Maximizing the leakage resistance will also reduce the energy loss in the capacitor.

The temperture stability of the capacitor's value needs to be as high as possible in a sample-hold's hold capacitor. The temperature stability of a capacitor is usually specified as percent change per degree celsius. The errors caused by a varying hold capacitor value are mostly in the sample-hold step and in the droop rate. Since each of these errors can be calibrated out of a dedicated ADC, any change in these sample-hold parameters with temperature will cause output errors from the ADC.

Table B.I

Capacitor Dielectric Comparison

Dielectric	Glass	Polyester	Polycarbonate	Parylene	Polypropylene	Polystyrene	Teflon
Parameter/ Characteristic							
DF, %	0.1	0.3-1.0	0.1-0.3	0.1	0.01-0.03	0.01-0.03	0.01-0.03
DA, %	5	0.3-1.0	0.1-0.3	<0.1	<0.1	<0.1	<0.1
IR, 25 C	High	Med/High	High	Very high	Very high	Very high	Very high
ΔDF/freq.	Very low	Medium	Medium	Low	Very low	Very low	Very low
ΔC/freq.	Very low	Medium	Medium	Low	Very low	Very low	Very low
ΔDF/temp.	Low	Med/High	Medium	Low	Very low	Very low	Very low
ΔC/temp.	Low	High, Non-linear	Med/Low	Low, linear	Med/Low	Low, linear	Low, linear
Stability	Excellent	Poor	Good	Excellent	Excellent	Excellent	Excellent
Tolerances Available, %	1-10	1-10	1-20	0.5-10	1-20	0.5-10	0.5-10
Range of Values	1-10,000 pF	1-10,000pF	0.001-5 uF	0.001-1 uF	0.001-5 uF	10 pF - 5 uF	0.001-5 uF
Relative Size of Higher Values	Large	Medium	Medium	Large	Large	Large	Large
Relative Cost	High	Lowest	Medium	High	High	High/low	Highest

Source: W. G. Jung and R. Marsh, "Selection of Capacitors for Optimum Performance - Part 2, Picking Capacitors," Audio, March 1980, p.56.

The dielectric absorption of the capacitor is one of the largest sources of error in any high resolution analog device. Dielectric absorption is a measure of a capacitors ability to remember previous voltage levels. The memory mechanism involves the polarization of the molecules in the capacitor's dielectric. If the capacitor is charged at some level for a relatively long period of time and then quickly shorted, not all of the polarized molecules in the dielectric will return to a random orientation during the shorting time. The polarized molecules will then create an electric field which will cause a voltage proportional to the previous charge level, the shorting time, and the the time since capacitor shorting began.

The dielectric absorption percentage is a method of comparing the magnitude of this effect in different dielectrics. The dielectric absorption percentage is the ratio, in percent, of the voltage to which the capacitor floats in some period of time after it has been shorted and open circuited, to the previous charge voltage. Care must be taken in comparing dielectric absorption percentage figures from different sources since the time during which the capacitor's voltage is allowed to float seems to vary between sources. As an example, the dielectric absorption percentage values given in [date1] page 172 vary by an order of magnitude from those given in Table B1.

Equation B1 [1] shows that the capacitor's voltage, V_C, is proportional to the charge voltage and the natural logarithm of the total time and the shorting time.

$$V_C = \Delta V * \ln(t_T / t_S) \qquad (B1)$$

where: $\Delta V = DA * V_O / \ln(t_T / t_S)_{DAT}$,

V_c is the capacitor voltage,

DA is the Dielectric absorption ratio,

V_o is the initial charge voltage,

t_T is the total time since the shorting began,

t_s is the shorting time.

$(t_T/t_s)_{DAT}$ is the ratio of total to shorting times used in measuring the dielectric absorption ratio, a constant.

The values for t_T and t_s are equivalent to the sum of the sample and the hold times, and the sample time respectively. From this relation it can be seen that the voltage error caused by the dielectric absorption effect can be minimized by making the sample mode duty cycle as large as possible.

Since the values for the dielectric absorption are not usable in calculating the capacitor's voltage unless the test conditions are given it is usually necessary to use experimental data to determine the magnitude of the error caused by the dielectric absorption. One of the best test circuits for examining the effect of dielectric absorption on sample-holds is given in an article by Robert A. Pease; Understand Capacitor Soakage to Optimize Analog Systems, EDN, October 13, 1982, pages 125-129. Figure B2 contains some of the results published in this article showing how the varying lengths of the sample and hold times affect the magnitude of the dielectric absorption voltage error.

In the report by R. A. Pease, the hold mode is ten times the length of the sample mode. In the track-and-hold designed for

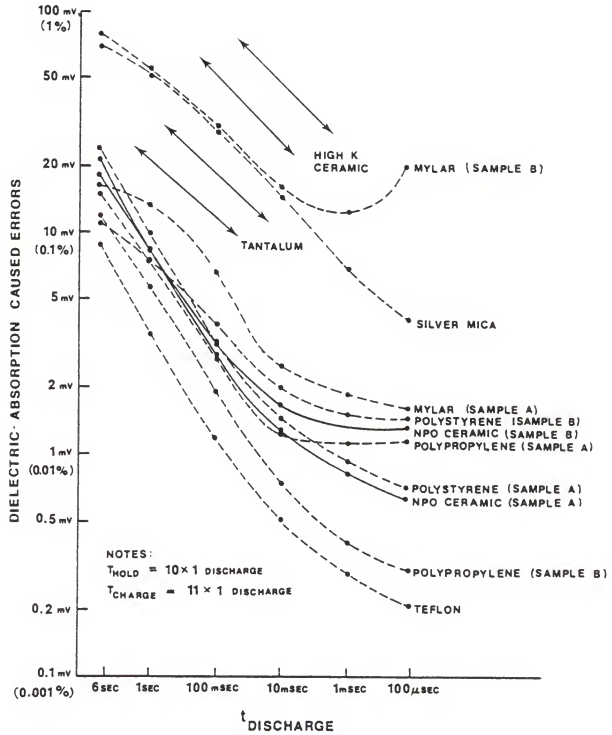


Figure B.1. Dielectric absorption errors as a function of discharge (sample) times.

From: R. A. Pease, *Understand Capacitor Soakage to Optimize Analog Systems*, EDN, pp. 125-129, October 13, 1982.

this paper this ratio is reversed with the sample time being seven or eight times as long as the hold time. Since the dielectric absorption error is proportional to the natural log of this time ratio, the track-and-hold used in this paper should have a dielectric absorption error that is only .13 of the magnitude shown in Figure B2, or an error of 50 microvolts for a sample time 10 milliseconds long. This error is well under one half the LSB of the ADC and should be acceptable.

Appendix C.

Comparison of Low Power Operational Amplifiers

There are several types of low power operational amplifiers available commercially today. The low power operational amplifiers can be divided in several ways, but perhaps the easiest method is to divide them by those which are programmable and those which are not. Once the operational amplifiers are so divided, further divisions can be made on the basis of technology used in construction and performance.

Many of the major analog semiconductor manufacturers have a version of the programmable operational amplifier, as shown in Table C.I. Table C.I shows some of the performance characteristics of each operational amplifier. This listing includes operational amplifiers with both bipolar (PMI OP 22, Motorola MC 1776), CMOS (TI TLC271) and combination technologies (RCA's "BiMOS" CA3440 and National's "BiFET" LF441.)

The advantages of the bipolar programmable operational amplifier include greater temperature stability, especially of the input bias currents and high gain. The "BiFET" types combine the extremely high input impedance of an FET input stage with the stability of bipolar amplifier and output stages. The CMOS programmable operational amplifiers have high input impedance, very low power consumption and the ability to operate very close to both voltage rails.

There are two methods for programming the operational amplifiers; the first using only a resistor, the second requiring a current source. Using a resistor to program the power level of

one of the programmable operational amplifiers is done by adding a resistor to the I_{set} pin to either ground or the negative supply. This programming method is simple and will provide good results where the operational amplifier can be used with the same performance parameters at all times. The second programming method involving the current source is achieved by the addition of an external transistor which will supply the desired set current. This method can give the designer the option of varying the operational amplifier's performance parameters by changing the transistor's bias and therefore the set current to the programmable operational amplifier.

Table C.I

Table of Parameters for Various Low Power Operational Amplifiers

Parameter	OP 20	OP 22	MC1776	TLC271	CA3440
Programmable	no	yes	yes	yes	yes
Bipolar	yes	yes	yes	no	no
CMOS	no	no	no	yes	no
Bipolar-FET	no	no	no	no	yes
V_{os} mV	.25	.1	2.0	3.0	0.8
I_{os} pA	1000	200	2000	1.0	2.5
I_B pA	12000	8000	15000	1.0	10
DC Gain dB	115	125	110	110	100
Band Width kHz	100	70	200	700	80
DC CMRR dB	90	115	90	88	90
DC PSRR dB	72	110	90	85	94
Programmable with set resistor		yes	yes	no	yes

The OP 22 programmable operational amplifier was chosen for use in the low power track-and-holds because of its very high gain, PSRR, and CMRR. The bipolar input stage of the OP 22 results in a higher droop rate for the track-and-hold because of the larger input bias current. The input bias current of a bipolar input stage is stable to within several tens of percent over the operational temperature range where CMOS operational amplifiers have input bias currents that may change by several magnitudes with temperature. Since stability in the droop rate was deemed essential to proper operation the advantages of a smaller droop rate at some temperatures was not used.

THE USE OF LOW POWER OPERATIONAL AMPLIFIERS IN TRACK-AND-HOLD AMPLIFIERS

by

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1984

Abstract

The development of a low power track-and-hold amplifier for low frequency, high resolution signal processing applications was investigated. Sample-Hold theory and the use of a track-and-hold as a sample-hold was researched. The use of low power operational amplifiers in the track-and-hold amplifiers to achieve the required power consumption and circuit performance was investigated. Three different track-and-hold circuit configurations were then constructed using the low power operational amplifiers. Test procedures for these high resolution track-and-holds were then developed and used to test their performance parameters. Of the three configurations tested the open-loop follower track-and-hold using the OP 22 operational amplifier and DG 309 analog switch gave the best results. This configuration is capable of being used with a 15 bit analog to digital conversion system at sample rates of up to 700 samples per second.